ABSTRACT

A field programmable gate array architecture comprises a plurality of horizontal and vertical routing channels each including a plurality of interconnect conductors. Some interconnect conductors are segmented by user-programmable interconnect elements, and some horizontal and vertical interconnect conductors are connectable by user-programmable interconnect elements located at selected intersections between them. An array of rows and columns of logic function modules each having at least one input and one output is superimposed on the routing channels. The inputs and outputs of the logic function modules are connectable to ones of the interconnect conductors in either or both of the horizontal and vertical routing channels. At least one column of random access memory blocks is disposed in the array. Each random access memory block spans a distance of more than one row of the array such that more than one horizontal routing channel passes therethrough and is connectable to adjacent logic function modules on either side thereof. Each of the random access memory blocks has address inputs, control inputs, data inputs, and data outputs. User-programmable interconnect elements are connected between the address inputs, control inputs, data inputs, and data outputs of the random access memory blocks and selected ones of the interconnect conductors in the horizontal routing channels passing therethrough. Programming circuitry is provided for programming selected ones of the user-programmable interconnect conductors to connect the inputs and outputs of the logic function modules to one another and to the address inputs, control inputs, data inputs, and data outputs of the random access memory blocks.